Wax 22193

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Packet Radio Temporary Note # 97

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SYNCHRONIZATION PREAMBLES

1.0 INTRODUCTION

Transmission over the UHF links in the ARPA network will require packet synchronization at the receive and repeater terminals. By the utilization of surface acoustic wave devices (SAWD's), chip synchronization is not required. There are several approaches to the packet synchronization problem which can be utilized. These approaches are discussed in varying degrees of depth below, from which the recommended approach is selected.

Several assumptions are made in the evaluation of the candidate preamble schemes. Some of these assumptions are:

1. The modulation will be minimum shift keying (MSK).
2. Code spread spectrum pulse width of $T_C = T_B/N$, where N is the number of chips per bit, while allowing the radiated power to be constant.
3. Minimum data rate of the order of 100 kbps.
4. Bit error probability of 10^{-5}.
5. The processing gain will be in the vicinity of 10 to 20 dB.

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Each of the approaches considered assumes that a bit is spread into 127 chips which make up a 127 chip maximum length sequence. Four preamble approaches are considered and compared. These approaches fall into two classifications: (1) Barker codes and (2) Repeat codes.

2.0 PREAMBLE SPECIFICATIONS

To begin a discussion of preamble detection, one must establish some preamble specifications. If we assume that a packet consists of 1,000 bits of data maximum, then a bit error probability of 10^{-5} results in a packet error rate of 10^{-2} without error detection and correction. Since error detection with automatic request for retransmission will be used rather than error correction, it would not be desirable that the packet error probability or retransmission probability exceed 10^{-2}. The preamble should have a detection probability at least as good and probably better than the packet detection probability. Therefore, the design goal for the probability of preamble detection will be 99.9%.

A frequently used relationship between false alarm probability and average time between false alarms is given by:

$$P_{FA} = \frac{1}{T_{FA} B}$$

where P_{FA} is the false alarm probability.

T_{FA} is the average time between false alarms.

B is the information bandwidth = 100 kHz.

Assume that a packet consists of 1,000 bits. Thus, a packet duration is 10 milliseconds. If we assume one false alarm for every 1,000 packet times, i.e., every 10 seconds, then $P_{FA} = 10^{-6}$. This will be the false alarm probability design goal.

For differentially coherent PSK on MSK modulation a 10.4 dB signal-to-noise ratio (E_b/N_o) is required to achieve a bit error rate (BER) of 10^{-5}. For this probability of bit error, 1% of the 1,000 bit packets will be in error. However, a reasonable approach is to assume a 50% probability of packet error in order to come up with the worst case preamble design. The 1,000 bit packet has a 50% probability of error for a BER = 7×10^{-4} corresponding to E_b/N_o = 8.2 dB. A 200 bit packet has a 50% chance of being correctly received for BER = 4×10^{-3} which corresponds to 6.5 dB. Since the preamble length is the same for either packet size, the design goal will be to provide a preamble having a 99.9% probability of detection in a worst case E_b/N_o environment of 6.5 dB. This margin can also be applied to some system degradations such as timing errors, frequency offset, doppler, and sidelobes.

3.0 PREAMBLE ANALYSIS

3.1 Coherent Combining

The required preamble length and E_b/N_o to achieve the probability of detection of .999 and probability of false alarm of 10^{-6} is a function of the detection technique. Coherent combining of the preamble yields the best results. The probability of missing the preamble versus the signal-to-noise ratio for a bit is plotted in Figure 1 with the number of bits in the preamble as a parameter.

Also, the false preamble probability os 10^{-6}. The results show that 8 bits are required to achieve the design goals. The analysis deriving these results is given in Appendix A.

The coherent combining of the bits at the output of the SAWD is difficult. The combining accuracy is a function of the IF frequency and must be less than 1 nanosecond. The delay can be achieved with a surface wave device matched to the MSK SAWD.

3.2 Non-Coherent Combining

If the preamble bits are combined non-coherently, additional bits are required to achieve the same design goals. This is demonstrated with Figure 2 where the number of preamble bits required for a missed preamble probability of 10^{-3} is plotted versus the signal-to-noise ratio. The curves are shown for two values of probability of false alarm 10^{-3} and 10^{-6}. To achieve the design goals stated above requires a minimum of 13 bits of preamble. The derivation of these curves is given in Appendix B. In order for the analysis to be tractable some simplifying assumptions were made. For low values of BT the results are a few tenths of a dB pessimistic.

3.3 Post Detection

A detection decision is made on each bit for the third approach. To exceed the threshold for detecting the preamble requires that M out of N bits are received correctly. In one case considered, a Barker code is used to achieve both bit timing and the sync preamble. The 13 bit Barker code is followed by another 13 bit Barker code where each bit of the second code is reversed in sign. For 26 bits of preamble 21 or more must agree with the stored reference at the receiver to achieve the design goals. The results are plotted in Figure 3. The derivation of these curves is given in Appendix C.

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4.0 PREAMBLE APPROACHES

4.1 Introduction

Four different preamble approaches are discussed in this section. Some of the advantages and disadvantages of each approach will be given. There are many variations and implementation approaches which can be suggested. In the interest of getting at the underlying principles, just a few of the possibilities are shown.

For each of the preamble approaches considered each bit consists of 126 or 127 chips, the exact number depending upon the code used to select the chips. The basic preamble principles hold independent of the number of assumed chips per bit.

4.2 Barker Preamble With Coherent Detection (Coherent Combining)

One of the most classic approaches is the use of the Barker sequences for preamble detection. This family of sequences is characterized by:

$$R(k) = \begin{cases} N & k = 0 \\ \pm\ 1,0 & k \neq 0 \end{cases}$$

where R (k) is the autocorrelation function and N is the number of bits comprising the sequence. The size of the family is restricted since there are no more than nine known Barker sequences. The Barker code coming closest to satisfying the requirements stated above is of length N = 7. The next largest Barker sequence is of length N = 11. For N = 7 its sequence is given by:

+++--+-

This sequence gives a ratio of 16.9 dB between the peak and the sidelobes. A plot of the autocorrelation of the Barker sequence illustrating this is given in Figure 4. Each bit of the Barker sequence consists of 127 chips from a 127 chip maximum length shift register. If the Barker bit is positive, the 127 chip sequence is transmitted. If the Barker bit is negative, each chip of the 127 chip sequence is inverted. A possible preamble detector implementation is shown in Figure 5. Each SAWD is matched to one bit of the Barker code. The first SAWD has the cosine pulse inter-digital transducer in addition to the 127 taps corresponding to the 127 chips. For further details on possible SAWD implementations of MSK detectors, see Appendix C.1. The outputs of the 7 SAWD's are summed coherently, amplified and compared to a threshold. A level sensing circuit establishes the input signal level and normalizes the output of the video amplifier so that a fixed threshold V_T can be used. When this threshold is exceeded, the presence of the preamble is indicated. A pulse is triggered at the time the threshold V_T is first exceeded. The pulse is terminated when the signal falls below the threshold. The center of this pulse is then estimated which establishes the bit timing for the remainder of the packet. The preamble accomplishes two functions: (1) It establishes bit timing and, (2) it indicates the start of the message. A discussion of the accuracy to which the bit timing can be estimated is given in Temporary Note #33. The following expression was derived for the time of arrival variance for a practical center pulse estimator:

$$\sigma_T^2 = \frac{\gamma^2}{2\,(2\,E/N_0)}$$

where E/N_0 is the signal to noise ratio and γ in the chip duration. For γ = 79 nanoseconds and E_b/N_0 = 6.5 dB we get σ_T = 18.6 ns.

From the autocorrelation function of the preamble (Figure 4) it can be seen that multipath which is delayed by 100 ns relative to the received signal will be rejected. Since coherent MSK detection is used in this example there is a 180° phase ambiguity of the chips and bits. Therefore, the received cross-correlation pulse at the output of the SAWD will be either positive or negative. This presents no problem as long as we are not detecting data since the output of the envelope detector is always positive.

As noted above, the peak-to-sidelobe ratio is 16.9 dB (7:1). The sidelobes, in effect, add to noise, thereby reducing the effective signal/noise ratio by 1/7th (1.34 dB).

One practical shortcoming is in the implementation of this approach as it requires seven 10usec SAWD's in cascade, each of which has from 10 to 30 dB insertion loss. Longer SAWD's can be used with more taps on each SAWD. The practical limitation with today's technology is about 40usec.

With the use of the 7 bit Barker code described above, the design goals are missed only by 0.5 dB (the design goal required 8 bits). However, the next shortest Barker code is 11 bits long.

Another disadvantage is that the effects of doppler shift and frequency errors are cumulative through the entire preamble. Thus, the coherent technique is much more sensitive to such offsets than a non-coherent combining technique.

One feature of this technique is that the first two SAWD's could be used for detecting differentially coded MSK data signals. Also, the derivation of bit timing and the end of preamble or start of message indication do not have to be derived separately.

4.3 Barker Preamble With Differentially Coherent Detection (Coherent Combining)

Another Barker preamble approach is shown in Figure 6. This approach requires only two SAWD's while yielding performance close to that of the optimum approach discussed above. Differential MSK modulation and detection are employed. The details of the modulation technique are discussed more completely in Appendix C.1 on modulation approaches.

The MSK SAWD's are 1 bit time long or 10 μsec. In essence they are filters matched to the spread signal on a bit basis. They remove the pseudo-noise spreading. A baseband preamble is obtained at the output of the comparator. Although a second analog matched filter matched to the 7 bit Barker sequence would be optimal, a close approximation can be obtained by limiting the baseband signal as shown and sampling at a high rate relative to the bit rate. Ten samples per chip would be realistic. This 8890 (10 x 127 x 7) length sequence of samples is then correlated in a digital matched filter with the stored sequence. It may be possible to implement this operation with a high speed ROM. The summer consists of counting the pairs of bits which are alike. When the digital counter exceeds a predetermined threshold value the preamble presence is established. Bit timing can also be derived in a manner similar to that discussed above.

The advantage of this approach is the reduction in the number of SAWD's. Another advantage is that since the bits are encoded differentially the bit detection circuitry can be used to detect subsequent message data bits without the need for separate data detection circuitry.

is to use four 10μsec SAWDS similar to that shown in Figure 5. A threshold V_{T2} is used to indicate the presence or absence of the code at the sample time. If the output exceeds the threshold V_{T2} at sample time, then the end of preamble is indicated and data detection commences.

This approach is relatively straightforward. It requires a few extra preamble bits because the detection process is divided into two parts.

4.5 M Out of N Preamble Detector (Post Detection Combining)

An M out of N preamble detector, where N is the number of bits in the preamble and M is the number of bits which must match to detect the preamble, is shown in Figure 9A. The preamble length N is 26 bits. The preamble consists of a 13 bit Barker code followed by an inverted 13 bit Barker code. The Barker code and its inverse is given by:

+++++--++-+-+ Barker

$\overline{\text{-----++--+-+-}}$ $\overline{\text{Barker}}$

The MSK detection process can be implemented as shown using a SAWD. The details of this implementation approach are discussed in the Modulation Waveform paper, Appendix C.1.

In this preamble technique the bit integration occurs after the bit decisions are made. At the detector output, point A of Figure 8, the waveforms are correlation pulses of 4 chips duration (316ns) occuring at the bit rate (10μsec intervals). The pulses are either positive or negative. A positive pulse exceeding the threshold yields an output pulse from the upper comparator (C). This pulse

is shifted asynchronously into the register. An initial estimate of bit timing is also derived from this pulse which is used to clock the register at subsequent bit intervals. If the pulse at the next bit sampling interval is positive and exceeds the threshold, it is shifted into the register. If the pulse is negative an output is obtained from the lower comparator. At the bit sampling interval this pulse is shifted into the register as a logic "0". The matched filter consists of a shift register and taps with each tap weighted by either a "one" or a "zero" in accord with the Barker code. One digital implementation approach is shown in Figure 9B. The two sums compute the number of matches and mismatches between the incoming data and the locally stored code sequences. The difference between the two outputs is compared against a threshold. When the threshold is exceeded an end of preamble (EOP) is obtained. If the register contains all zeroes and the 26 bit Barker, Barker code is received, the difference between the two summers of the digital matched filter (point P on Figure 9) follows the correlation function shown in Figure 10. The correlations are separated by the bit interval. Without any errors the output is always negative or zero until the preamble lines up exactly in the register. At this time the output is 26 units.

The expected performance obtained with this preamble approach is calculated in Appendix C. The results are plotted in Figure 3. The probability of a false alarm and the probability of a false preamble are plotted as a function of the threshold. In this analysis two thresholds are involved. The first one is used for the detection of the bits and the second for the detection of the preamble. The probability of a false alarm is not a function of the signal-to-noise ratio. The probability of a missed preamble is a function of the signal-to-noise ratio and is plotted for an SNR of 7.4 dB and 6.5 dB. If the preamble is set to 21, the probability of a false alarm is 10^{-7} and the probability of a missed preamble is 10^{-3} for a 6.5 dB SNR. This meets our design objectives.

One of the disadvantages of this approach is the length of the required preamble when compared with the approaches discussed previously.

An advantage is the relatively simple implementation requirement. The basic speed of the detector is at the bit rate with the exception of a counter in the center of pulse estimator which will operate from 5 to 10 times the chip rate. The basic SAND detector is used for detecting both the preamble bits and the subsequent data bits. The bit timing sampling pulse is derived simultaneously with the receipt of the preamble. A continuously improved bit timing estimate during the preamble enables a continuous improvement in the performance of the detected preamble bits.

4.6 Alternate Bit Timing Recovery Approach

Another way of acquiring bit synchronization which can be applied to any of the above preamble approaches is by using a conventional analog phase-lock-loop. A VCO is phase-locked to the incoming envelope detected correlation peaks which occur at the bit rate. The correlation pulses sample the phase of the local 100 kHz reference and hold the sample value. This sample value is filtered and the output is the control voltage for the VCO. After the VCO is locked to the correlation peaks, its timing is transferred to a counter derived from a stable clock. A method of implementing this technique is shown in Figure 11.

For this phase lock-loop, Hoffman's** analysis for transient response is shown in the table below. A loop bandwidth (ω_n) of $2\pi 16$ kHz is assumed for a phase-lock loop with 100 kHz reference frequency. This assumes AGC has been set and no noise is present.

** "Phase-Lock Techniques" by F. M. Gardner, p. 34.

PHASE ERROR	FREQUENCY LOCK TIME ($\omega_n t$)	PHASE TRANSIENT TIME $\Delta=\omega_n, \zeta = 1$ ($\omega_n t$)	TOTAL ($\omega_n t$)	BITS REQUIRED, NO NOISE $\omega_n = 2\pi 16$ KHz
10 ns → .36°	2	8.5	10.5	11
28 ns → 1°	2	7	9	9
100 ns → 3.6°	2	5.5	7.5	8

For noise, no analysis is available to calculate transient time. For S/N 10 dB, doubling the number of bits required seems appropriate; i.e., up to 22 bits might be required. AGC is assumed before phase locking. Of course, the phase-locking acquisition can occur before AGC is finally settled out.

Ten (10) ns of phase error corresponds to .4dB degradation point for ideal sampling with timing offset for maximum likelihood detection. One-hundred (100) ns corresponds to $2T_c$ windows peak and store detection worst case where .5 dB degradation is seen. A 10 ns phase error requirement also places a stringent requirement on DC phase drift of the phase detector and counter circuits used. Strobing a counter with 10 ns increments requires clocks and counters operating in excess of 100 MHz.

Ten (10) ns requirements on timing is possible, but difficult, either with phase-locking or with SAWD's matched for preamble timing and detection. Therefore, if this approach is to be used, the window detecting method is recommended.

5.0 COMPARISON OF PREAMBLE APPROACHES

Figure 12 contains some parameters which are important for deciding which preamble approach is most desirable for the ARPA Packet Radio Network. The four preamble approaches are compared on the basis of performance and equipment complexity. Based on the probability design goals, the length of the preamble is different for each approach operating in the same signal-to-noise environment. The best performance is denoted by 1 and the poorest performance by 4. One should be cautioned that there may be other system factors which were not considered in this paper that may influence the selection of the length of the preamble.

Several approaches are possible for deriving bit timing. One approach uses a bit timing loop as discussed in 4.6. Another uses a time of arrival estimator. The objective is to estimate the time of occurrence of the correlation peak. Potentially the bit timing loop yields superior tracking performance. Both techniques can be applied to any of the preamble approaches discussed above. However, the longer preambles have the advantage of yielding more accurate bit timing estimates. On the basis of these arguments, the M out of N preamble technique can yield the best bit timing accuracy at the end of the preamble.

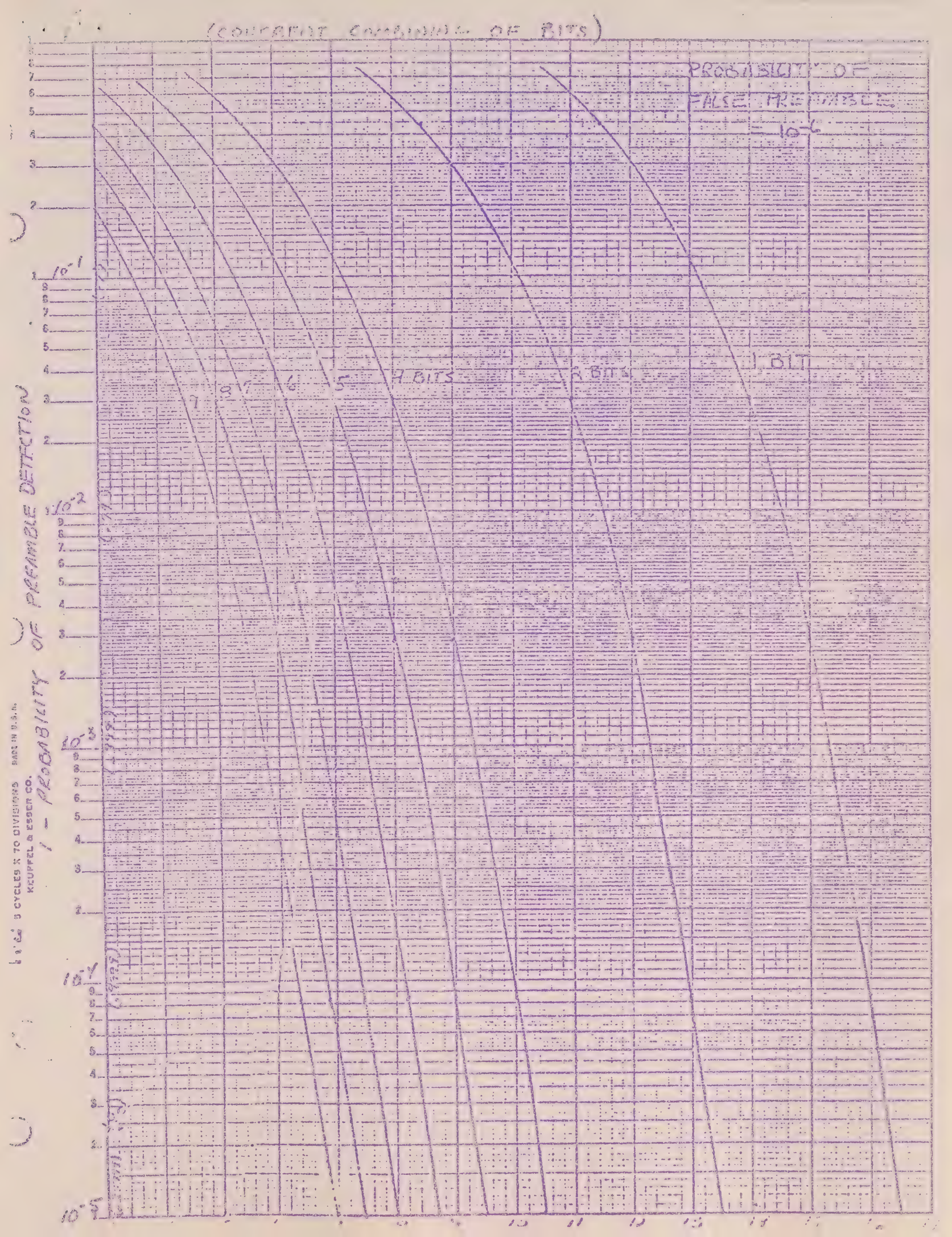
Multipath rejection is related to the width of the autocorrelation pulse and the sidelobe energy. Since the autocorrelation pulse width is identical in all approaches, only the sidelobes are of concern in this analysis. The sidelobe energy is greatest for the repeat preamble technique. The peak to sidelobe ratio is larger for the M out of N preamble detector than it is for the two coherent 7 bit Barker preamble approaches. Therefore, the multipath rejection is greater for the M out of N technique.

Doppler and frequency offset tolerance is related to the length of the SAWD and whether successive bits are combined coherently or non-coherently. The M out of N preamble technique gives the greatest tolerance because each bit is detected and then successive bits are accumulated. Thus, the phase error is accumulated over only a single bit (10μsec). One approach to solving the problem should the frequency error be excessive over a 7 bit interval is to estimate the frequency error and compensate for it at the injection frequency of the local oscillator. This adds to hardware complexity.

The equipment complexity comparison is subjective and was related largely on the basis of the number of SAWD's required and their design requirements.

One significant feature of several of the approaches discussed is the hardware commonality with the message demodulator. In the case of the second and fourth approaches listed in Figure 12, the MSK demodulators are identical for both the preamble and data. Some additional hardware is necessary for detecting the preamble.

On the basis of this tradeoff study, it is clear that the M out of N detector preamble with the 13 bit Barker followed by 13 bit inverted Barker is the recommended approach. One of the basic assumptions of this analysis is that the six tradeoff parameters considered are the most critical and that they are of equal importance.


(COHERENT COMBINING OF BITS)
PROBABILITY OF FALSE PREAMBLE = 10^{-6}
1 BIT
8 BITS
16
32
64
1 − PROBABILITY OF PREAMBLE DETECTION
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}

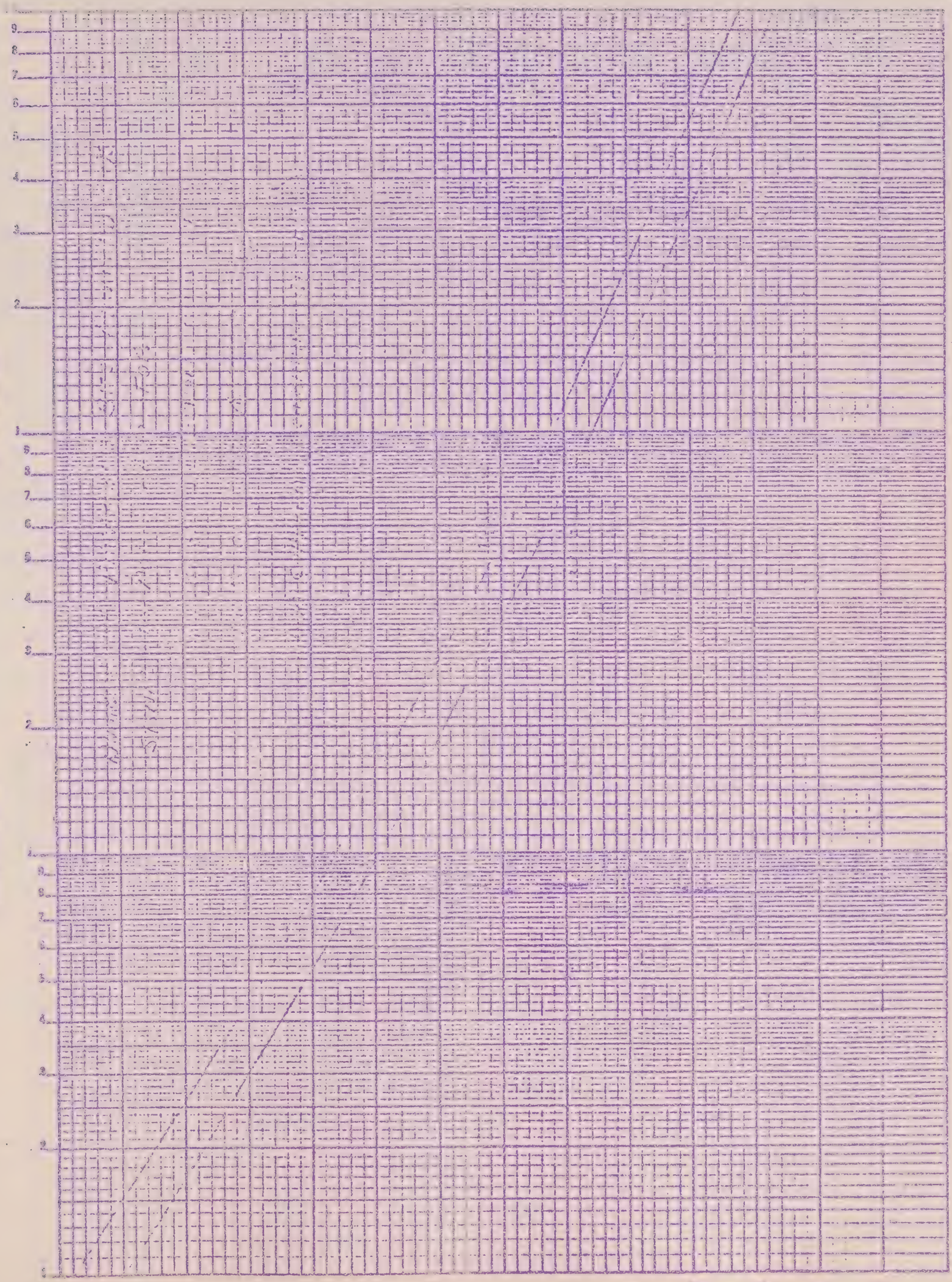
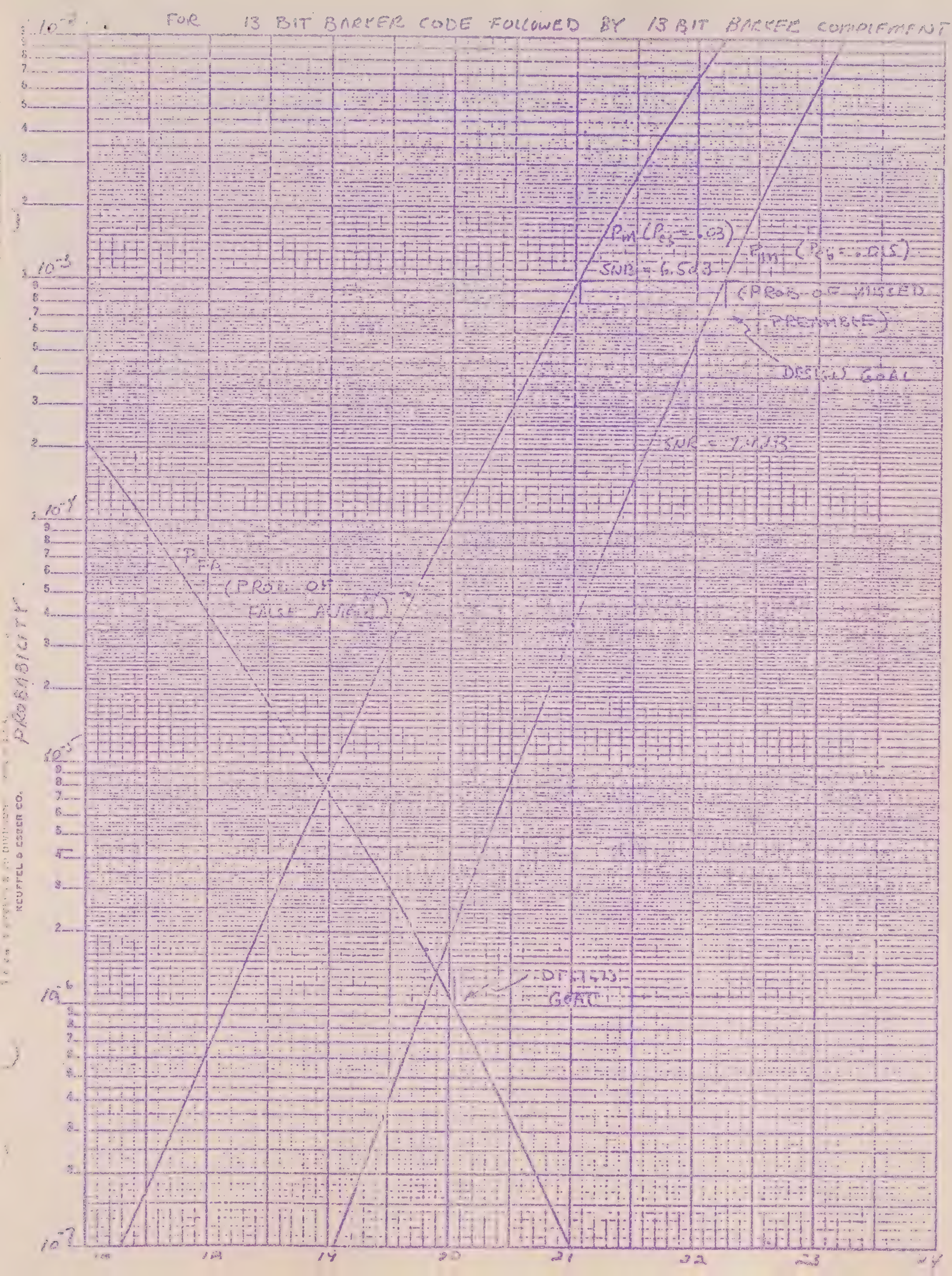


FIGURE 2

KE 359 SEMI-LOGARITHMIC 46 5493
5 CYCLES X 70 DIVISIONS MADE IN U.S.A.
KEUFFEL & ESSER CO.


FOR 13 BIT BARKER CODE FOLLOWED BY 13 BIT BARKER COMPLEMENTED
P_M (P_{FA} = .03)
SNR = 6.5 dB
P_M (P_{FA} = .01)
(PROB OF MISSED PREAMBLE)
DESIGN GOAL
SNR = 7 dB
P_{FA} (PROB OF FALSE ALARM)
DESIGN GOAL
PROBABILITY
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
18
19
20
21
22
23
24

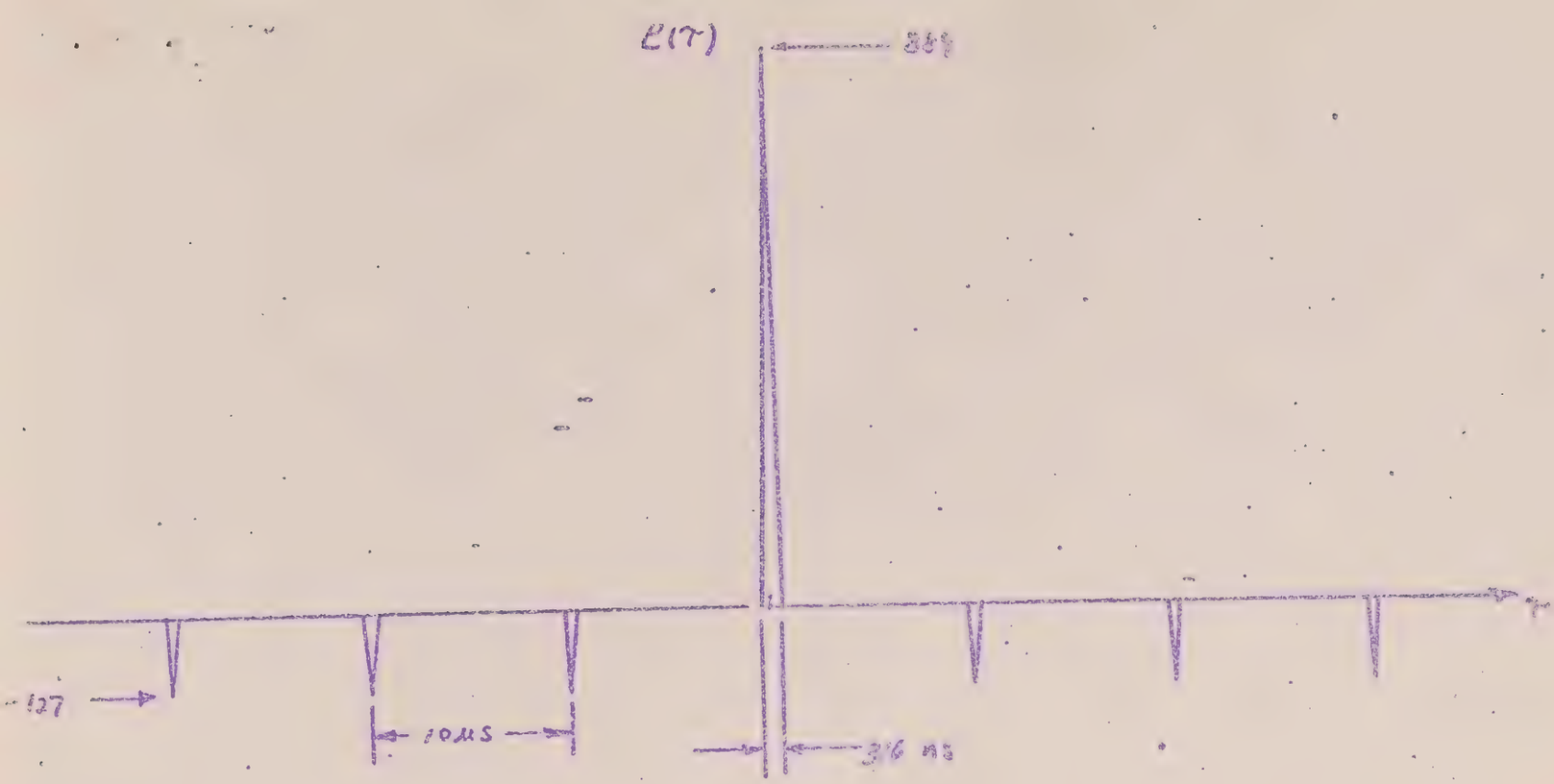


FIGURE 4 AUTOCORRELATION OF 7 BIT BARKER SEQUENCE WHERE EACH BIT CONSISTS OF 127 CHIPS OF A MAXIMUM LENGTH SEQUENCE AT 100 KBPS RATE.

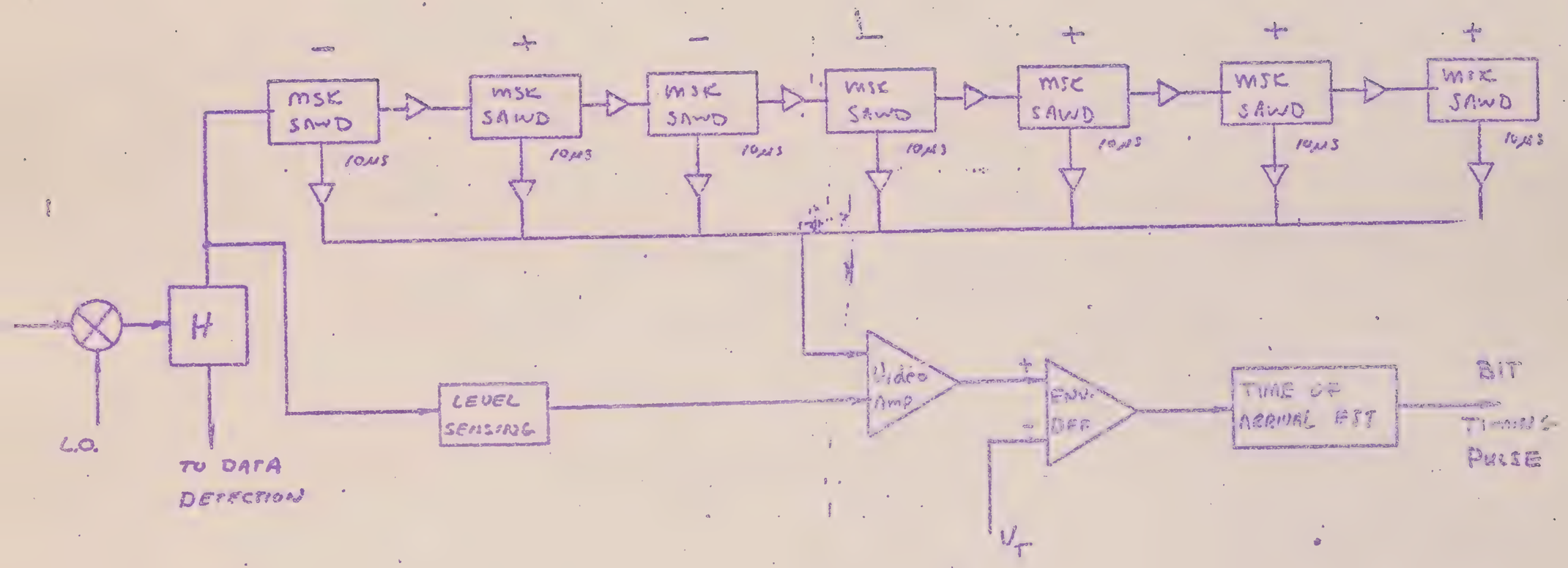


FIGURE 5 7 BIT BARKER PREAMBLE & BIT SYNC DETECTOR

COHERENT COMBING DETECTION

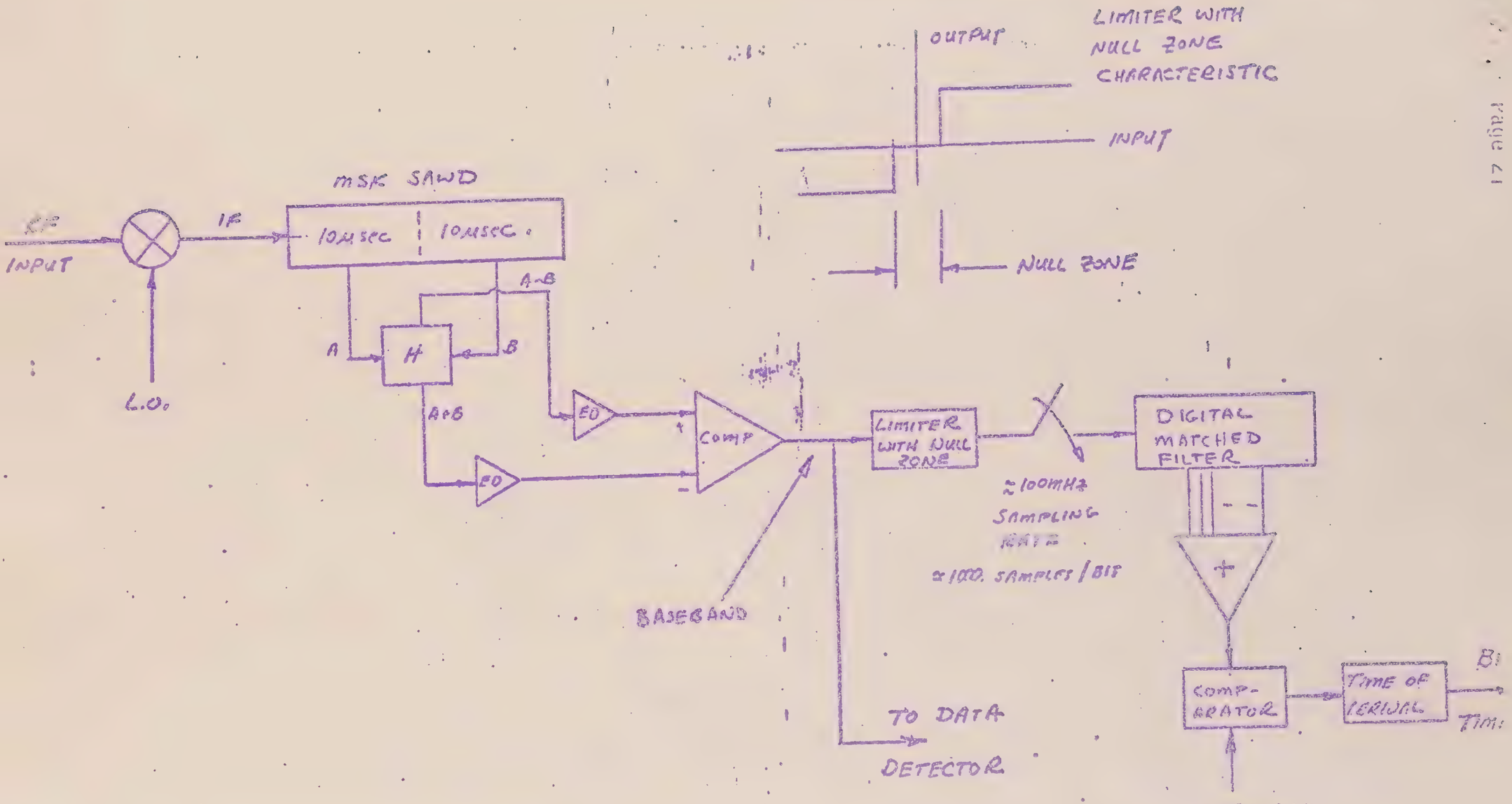


FIGURE 6 7 BIT BARKER PREAMBLE & BIT SYNC DETECTOR.

DIFF. COHERENT COMBINING DETECTION

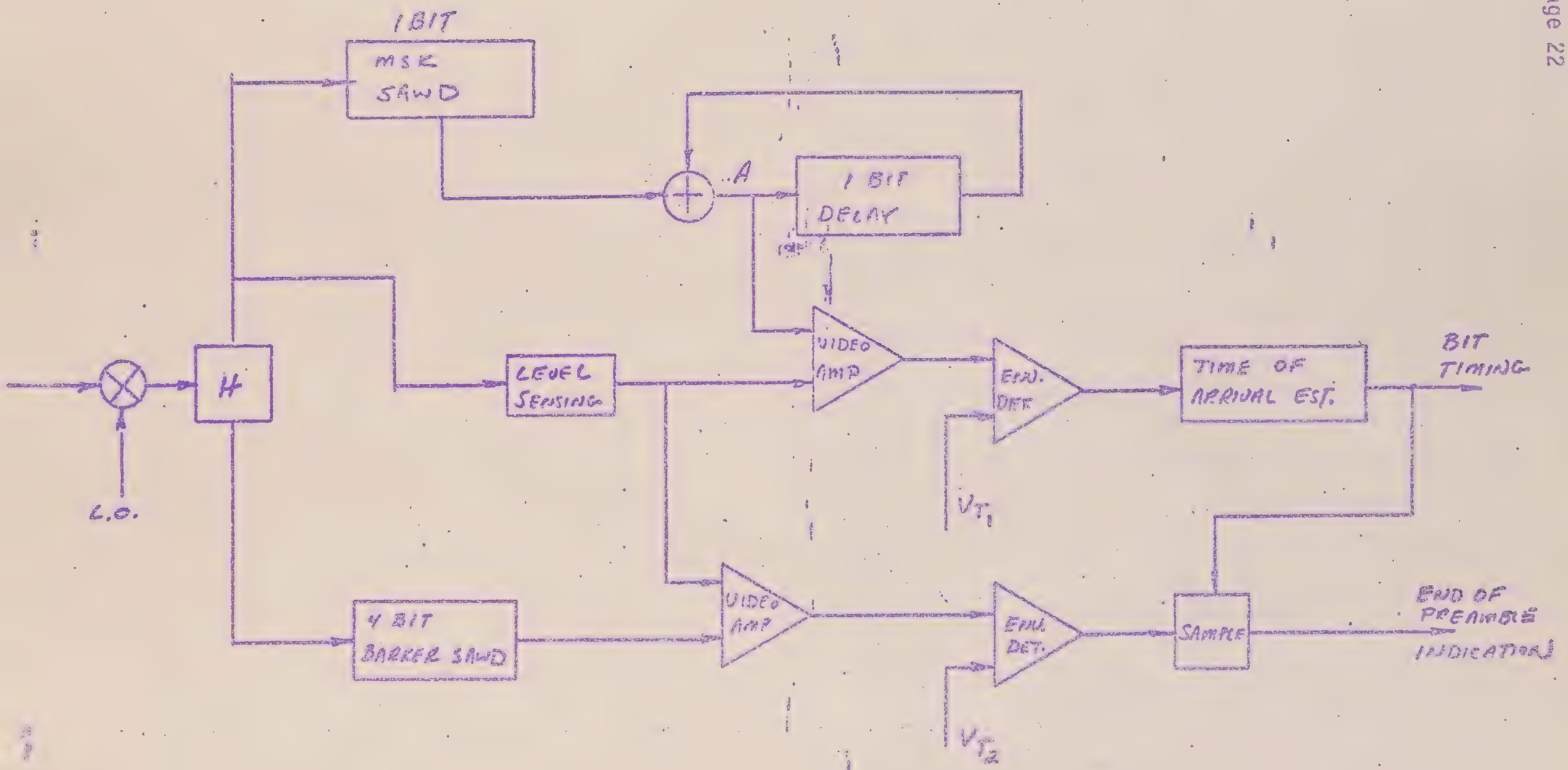


FIGURE 7 REPEAT PREAMBLE WITH END OF PREAMBLE DETECTOR

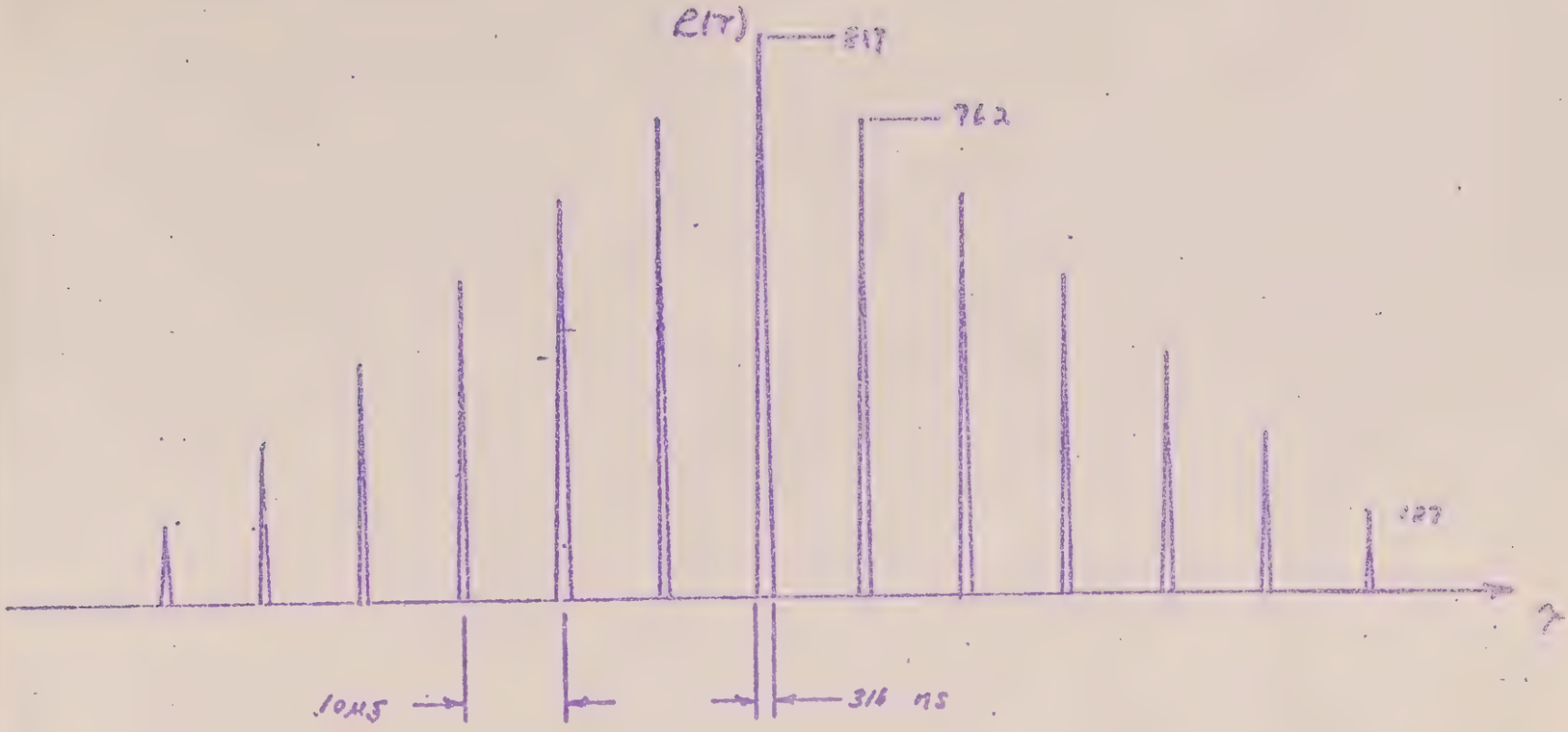
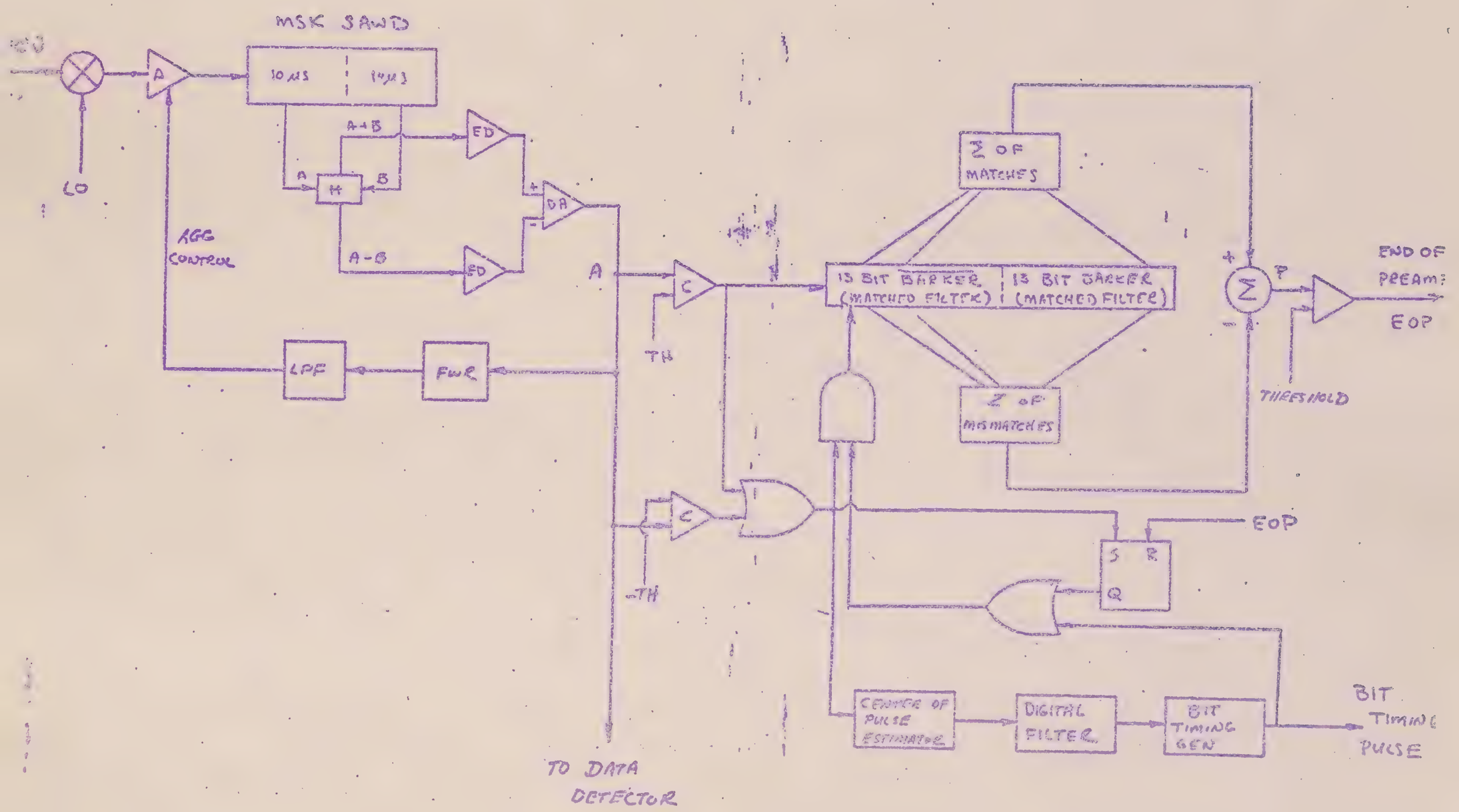
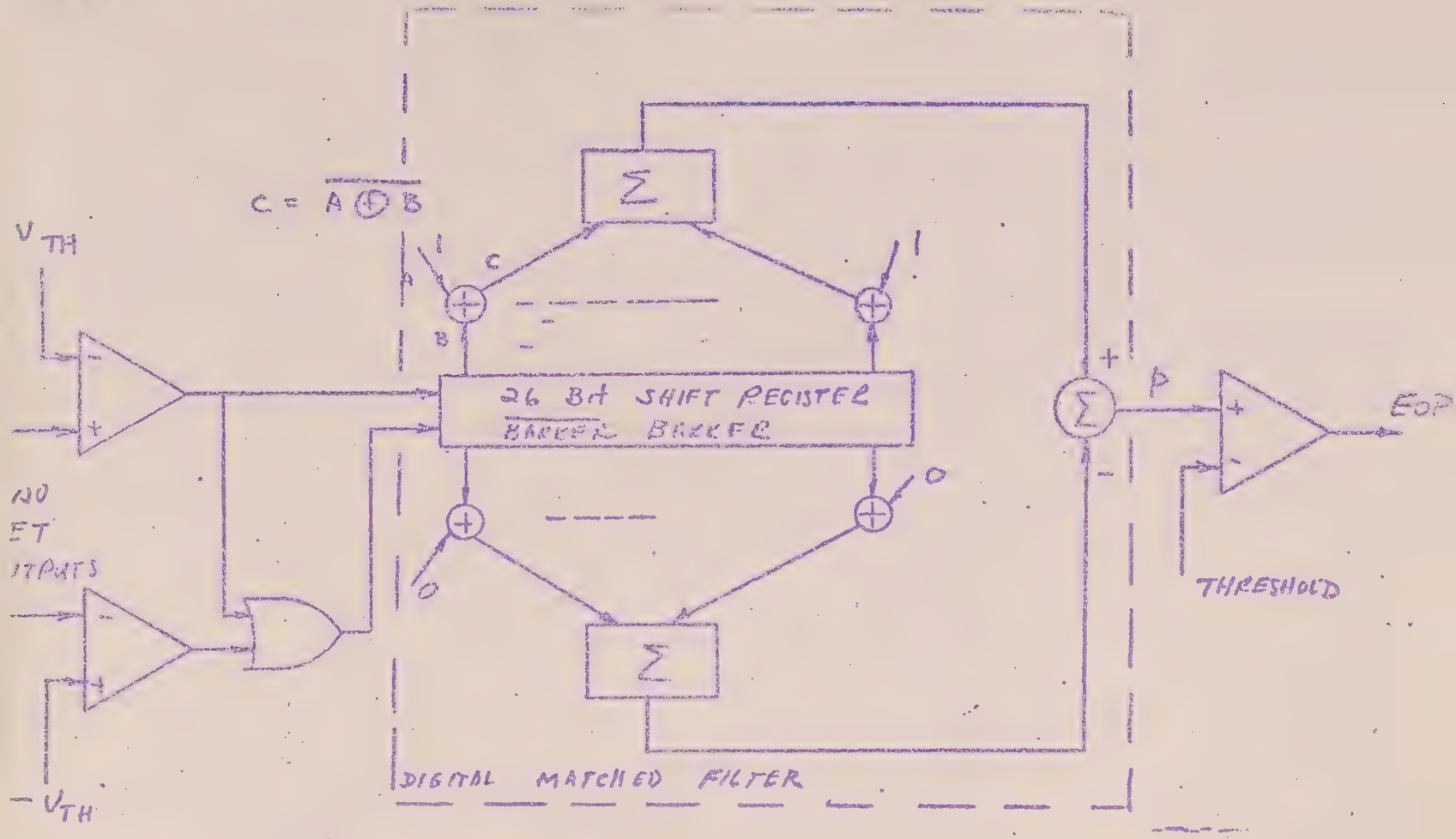


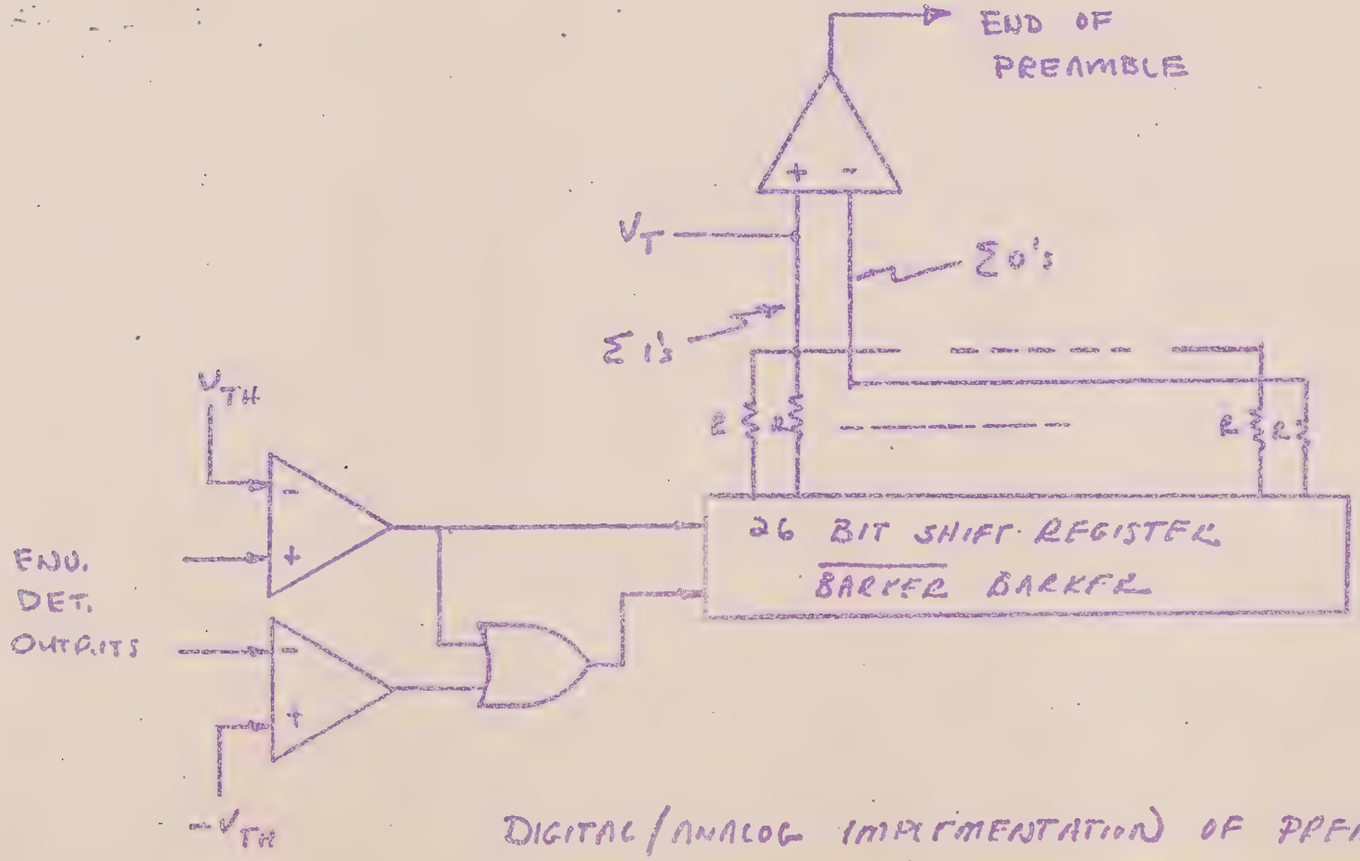
FIGURE 8 AUTO CORRELATION OF 7 "ONES" WHERE EACH BIT CONSISTS OF 127 CHIPS OF A MAXIMUM LENGTH SEQUENCE AT 100 KBPS

FIGURE 9A 13 BIT BARKER $\overline{\text{BARKER}}$ PREAMBLE & BIT SYNC DETECTOR
(NONCOHERENT DETECTION)





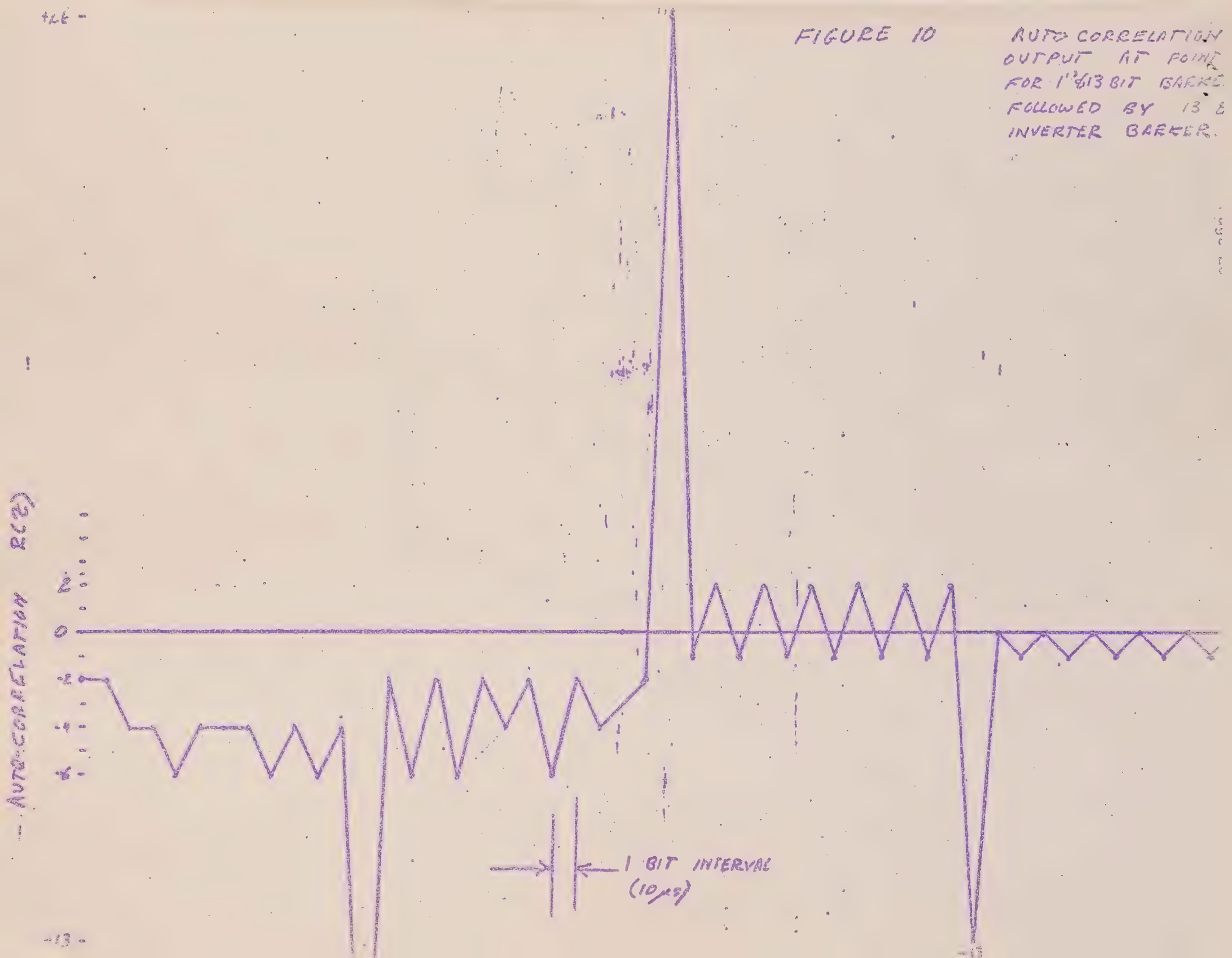
DIGITAL IMPLEMENTATION OF PREAMBLE FILTER



DIGITAL/ANALOG IMPLEMENTATION OF PREAMBLE FILTER

FIGURE 10

AUTO CORRELATION OUTPUT AT POINT FOR 1'S 13 BIT BARKER FOLLOWED BY 13 B INVERTER BARKER.



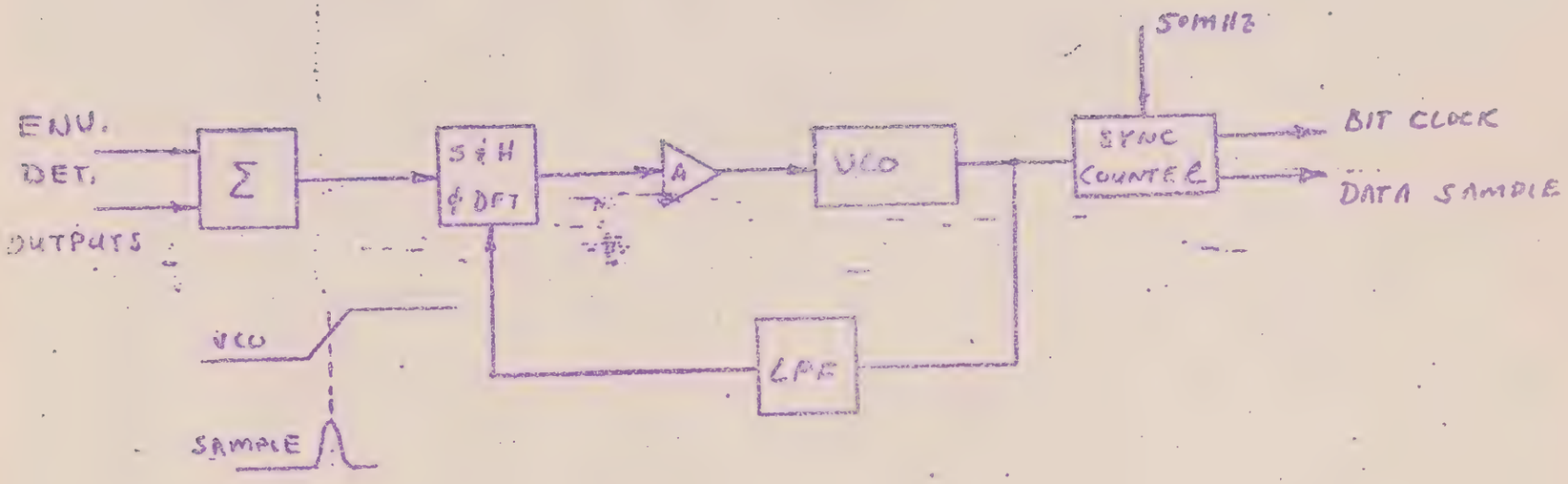


FIGURE 11 FUNCTIONAL DIAGRAM OF BIT SYNC LOOP

TRADEOFF PARAMETERS / PREAMBLE DETECTION TYPE	LENGTH OF PREAMBLE FOR FIXED P_D & P_{FA}	BIT TIMING ACCURACY	MULTIPATH REJECTION	DOPPLER AND FREQ. OFFSET TOLERANCE	EQUIPMENT COMPLEXITY	COMMONALITY WITH MESSAGE DEMODULATOR
BARKER PREAMBLE WITH COHERENT DETECTION	1	3	2	3	4	3
BARKER PREAMBLE WITH DIFF. COHERENT DETECTION	2	4	2	3	2	1
REPEAT PREAMBLE DETECTOR	3	2	3	2	3	2
M OUT OF N PREAMBLE DETECTOR	4	1	1	1	1	1

EVALUATION SCALE: 1 MOST DESIRABLE
TO
5 LEAST DESIRABLE

FIGURE 12

Appendix A

This appendix gives a summary of the analysis used to derive the detection probabilities of Figure 1. For a perfect envelope detector the probability of detection is

$$P_D = Q\left(\sqrt{\frac{2P_S}{\sigma^2}}\ \frac{T}{\sigma}\right)$$

which is the Marcum Q function where P_s is the power in the carrier sinewave at the detector input, T is the bit length and σ^2 is the noise power. The derivation of this is shown in Appendix B. The improvement in signal-to-noise ratio when n pulses are integrated with ideal predetection integration is n-times the signal-to-noise ratio of that for a single pulse. Therefore, 10 log n less signal-to-noise ratio is required in dB for n pulses combined coherently before detection.

Appendix B.

A model of the preamble detection circuitry is shown in Figure B1. The local code is cross-correlated with the incoming signal in a SAWD. The SAWD performs the function of a modulator and an integrator. The effective bandwidth of the SAWD is $B = 1/T_B$ where T_B is the integration time. The incoming signal itself was spread to a bandwidth $W = 1/T_c$, where T_c is the code chip duration. After the integration for time $T = NT_B$, where N is the number of bits which are coherently added, the signal is envelope detected and applied to a threshold device for a synchronization decision.

The time required to achieve bit synchronization (i.e., for the detected output to exceed the threshold) is a function of the signal-to-noise ratio, the desired detection probability, P_D and the false alarm probability, P_{FA}. The probability densities of the noise and the signal plus noise required to calculate these probabilities depend upon N. For N = 1, the probability density functions (P.d.f.) at the envelope detector output are Rayleigh and Rician, respectively. For $N \geq 8$ the probability density functions can be approximated by Gaussian densities for both noise and signal plus noise.

Consider first the case for N = 1. If the detector is assumed to be a perfect envelope detector the p.d.f. of the output noise in the absence of a signal (i.e., in the absence of sync) is Rayleigh. Hence, the probability of false alarm is:

$$P_{FA} = \int_{T}^{\infty} \frac{v}{\sigma^2} \exp\left(-\frac{v^2}{2\sigma^2}\right) dv \qquad (1)$$

$$= e^{-T^2/2\sigma^2}$$

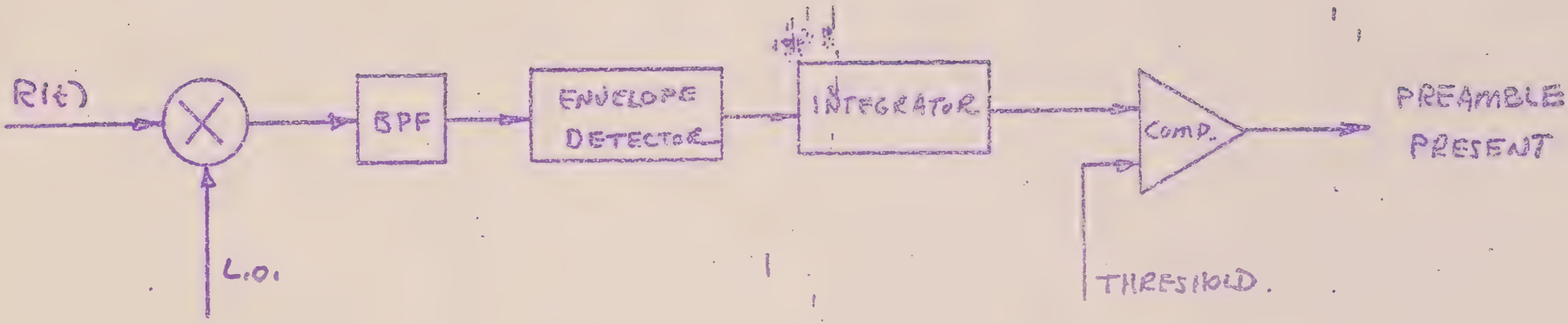


FIGURE B1 PREAMBLE DETECTION MODEL

when T = threshold voltage

σ^2 = N_0B = input noise power

for P_{FA} = 10^{-6}, we find that $T/\sigma = 5.26$ and

P_{FA} = 10^{-3}, we find that $T/\sigma = 3.72$

The p.d.f. of the detector output when one is within the two chip synchronization window is Rician. Hence, the probability of detection is

$$P_D = \int_T^\infty \frac{V}{\sigma^2} \exp\left(\frac{V^2 + 2Ps}{-2\sigma^2}\right) I_o\left(\frac{V\sqrt{2Ps}}{\sigma^2}\right) dV \qquad (2)$$

where Ps is the power in the carrier sinewave at the detector input. This is the Marcum Q function.

$$P_D = Q\left(\sqrt{\frac{2Ps}{\sigma^2}}, \frac{T}{\sigma}\right) \qquad (3)$$

for $P_{FA} = 10^{-3}$ so that $T/\sigma = 3.72$, we find that $P_D = 0.999$

for $P_s/\sigma^2 = 22.5$

Hence, the predetection SNR is:

SNR = 13.5 dB, $P_{FA} = 10^{-3}$, $P_D = 0.999$

For large BT products, i.e., for large N, we may use the central limit theorem to approximate the p.d.f. as Gaussian, both in and out of synchronism. Consider first the out-of-sync case and assume the detector is a square law device. The envelope detector is considerably more difficult to handle analytically; however, the results are very similar. The expected value of the detector output signal is:

$$E\{n\} = 2BT\,No$$

and the variance is

$$E\left\{n^2\right\} = \sigma_n^2 = (2BTNo)^2/BT = 4BTNo^2$$

The false alarm probability is therefore,

$$P_{FA} = 1/2\left[1 - \operatorname{erf}\left(\frac{T - E\{n\}}{\sqrt{2}\,\sigma_n}\right)\right]$$

and for $P_{FA} = 10^{-3}$ we have $\dfrac{T - E\{n\}}{\sqrt{2}\,\sigma_n} = 2.19$

If the codes are within sync (i.e., 2 chip window) the mean and variance of the detector output is:

$$E\{V\} = 2\,BTNo\left[1 + \frac{Ps}{BNo}\right] = 2BT.No + 2TPs$$

and $E\left\{V^2\right\} = \sigma_s^2 = (2BTNo)^2\left[1 + \dfrac{2Ps}{BNo}\right]/BT$

from which we get $P_D = 1/2\left[1 + \operatorname{erf}\left(\dfrac{E\{V\} - T}{\sqrt{2}\,\sigma_s}\right)\right]$

and for $P_D = .999$ we have $\dfrac{E\{V\} - T = 2.19}{\sqrt{2}\,\sigma_s}$

Now we are interested in solving for Ps/BNo = SNRi as a function of BT. We get

$$BT = \left(\frac{3.1 + 3.1\sqrt{1 + 2\,SNR_i}}{SNR_i}\right)^2$$

From this expression we can plot the results as given in Figure 2 for $P_{FA} = 10^{-3}$. A similar equation can be derived for different values of P_{FA}. The results are also plotted in Figure 2 for $P_{FA} = 10^{-6}$.

APPENDIX C

This appendix gives a summary of the analysis used to derive the preamble detection probabilities of Figure 3. In this approach a detection decision is made for each bit. To exceed the threshold for detecting a preamble requires M out of N bits being received correctly. If we assume that N "ones" are transmitted, then M-N errors are allowed in the received sequence. Therefore, the probability of detecting the preamble is

$$P_D = 1 - \sum_{i=1}^{M-N} \binom{N}{i} P_{eb}^{\ i} (1-P_{eb})^{N-i}$$

where P_{eb} is the probability of a bit error. For a 7.4 dB SNR and the threshold set for a probability of a false alarm per bit, $P_{FA_b} = .3$ per bit, the probability of a bit error is .015. With a SNR = 6.5 dB and the same P_{FA_b}, the probability of a bit error is .03. Without signal on the input a false alarm occurs with the occurrence of M or more "ones." Therefore, the false alarm probability can be written as

$$P_{FA} = \sum_{i=M-N}^{N} \binom{N}{i} P_{FA_b}^{\ i} (1-P_{FA_b})^{N-i}$$

Utilizing these two equations the results were plotted in Figure 3 for N = 26 and various values of M.